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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MATSUZAKI

Art Unit: 2816

Application No. 09/874,037

Examiner: H. Nguyen

Filed: June 6, 2001

Atty. Docket No. 100353-00064

For: SEMICONDUCTOR DEVICE, MODULE INCLUDING THE SEMICONDUCTOR DEVICE, AND SYSTEM INCLUDING THE MODULE

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

August 8, 2002

Sir:

In reply to the Office Action mailed May 8, 2002, please amend the above-identified application as follows:

IN THE TITLE:

Please amend the title to recite "A SEMICONDUCTOR PHASE ADJUSTMENT SYSTEM MODULE".

IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace page 9, paragraph 8, beginning at line 25 with:

a1

Fig. 7 is a block diagram of a module according to a first embodiment of the present invention. A memory module 14 shown in Fig. 7 includes, on a wiring board 160, memory devices 120 - 127 having an identical structure, a PLL circuit (PLL1) 15 for an input clock, a PLL circuit (PLL2) 16 for an output clock, data input/output terminals DQ and a clock input terminal CLK. A positive power source voltage VCC is applied, as an external instruction signal, to a dummy output enable terminal of the